

PART 1 of 2

2813 \$



DOCKET NO. CHEN 4-17-157

PATENT

#21
11-12-02
Muller

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Yuanning Chen, et al.

Serial No.: 09/597,076

Filed: January 20, 2000

For: PROCESS FOR FABRICATING OXIDES

Group No.: 2813

Examiner: Kielin, Erik S.

RECEIVED
NOV 12 2002
1C 2800 MAIL ROOM

Commissioner of Patents
and Trademarks
Washington, D. C. 20231

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 11/5/2002 (Date)
EDITH SHER
(Printed or typed name of person signing the certificate)
Edith Sher
(Signature of the person signing the certificate)
11/5/2002
(Date of Signature)

Sir:

THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

In accordance with 37 C.F.R. §1.56, and in accordance with the provisions of 37 C.F.R. §§1.97 and 1.98 and §609 of the Manual of Patent Examining Procedure, Applicant hereby makes an additional disclosure of the patents, publications and other information listed below and on the accompanying form PTO-1449, which references are considered to be potentially material to the patentability of the invention disclosed in the above-referenced application. Copies of the listed references are submitted herewith. Disclosure has been filed previously on April 30, 2001, August 29, 2001 and August 5, 2002.

11/08/2002 CCHAU1 00000088 09597076

01 FC:1806 180.00 OP

<u>U.S. Patent and Patent Application No.</u>	<u>Inventor</u>	<u>Date</u>
6,281,559	Yu et al.	August 28, 2001
6,281,140	Chen et al.	August 28, 2001
6,222,223	D'Anna	April 24, 2001
6,210,999	Gardner et al.	April 3, 2001
6,197,641	Hergenrother et al.	March 6, 2001
6,180,454	Chang et al.	January 30, 2001
6,083,836	Rodder	July 4, 2000
6,083,815	Tsai et al.	July 4, 2000
6,069,062	Downey	May 30, 2000
6,029,680	Hawthorne et al.	February 29, 2000
6,027,975	Hergenrother et al.	February 22, 2000
6,025,280	Brady et al.	February 15, 2000
6,020,247	Wilk et al.	February 1, 2000
6,008,128	Habuka et al.	December 28, 1999
5,972,804	Tobin et al.	October 26, 1999
5,968,279	MacLeish et al.	October 19, 1999
5,918,137	Ng et al.	June 29, 1999
5,913,149	Thakur et al.	June 15, 1999
5,891,809	Chau et al.	April 6, 1999
5,877,057	Gardner et al.	March 2, 1999
5,869,405	Gonzalez et al.	February 9, 1999
5,867,425	Wong	February 2, 1999
5,863,831	Ling et al.	January 26, 1999
5,821,158	Shishiguchi	October 13, 1998
5,814,562	Green et al.	September 29, 1998
5,757,204	Nayak et al.	May 26, 1998
5,629,221	Chao et al.	May 13, 1997
5,622,607	Yamazaki, et al.	April 22, 1997
5,619,052	Chang et al.	April 8, 1997
5,598,369	Chen et al.	January 28, 1997
5,567,638	Lin et al.	October 22, 1996
5,514,608	Williams et al.	May 7, 1996
5,371,394	Ma et al.	December 6, 1994
5,334,556	Guldi	August 2, 1994
5,153,701	Roy	October 6, 1992
5,089,441	Moslehi	February 18, 1992
5,077,691	Haddad et al.	December 31, 1991
5,016,081	Brown et al.	May 14, 1991
4,277,320	Beguwala et al.	July 7, 1981
09/597,077	Chen et al.	June 20, 2000
09/481,992	Chen et al.	January 11, 2000

<u>Foreign Patent No.</u>	<u>Country</u>	<u>Date</u>
JP 01 204435	Japan	August 17, 1989
EP 0 323 071	EP	July 5, 1989
EP 0 301 460	EP	February 1, 1989
JP 62 079 628	Japan	April 13, 1987
GB 2 056 174	UK	March 11, 1981

Publications

Ponomarev et al.; *High-Performance Deep SubMicron CMOS Technologies with Polycrystalline-SiGe Gates*; IEEE Transactions on Electron Devices, Vol. 47, No. 4; April 2000; pp. 848-855.

Lee et al.; *Enhancement of PMOS Device Performance with Poly-SiGe Gate*; IEEE Electron Device Letters, Vol. 20, No. 5; May 1999; pp 232-234.

Song et al.; *Ultra Thin (<20Å) CVD Si₃N₄ Gate Dielectric for Deep-Sub-Micron CMOS Devices*; Microelectronics Research Center, The University of Texas, Austin; 4 pgs.

Hattangady et al.; *Ultrathin nitrogen-profile engineered gate dielectric films*; Semiconductor Process and Device Center, Texas Instruments; 4 pgs.

Tseng et al.; *Reduced Gate Leakage Current and Boron Penetration of 0.18 μm 1.5 V MOSFETs Using Integrated RTCVD Oxynitride Gate Dielectric*; 4 pgs.

Hattangady et al.; *Remote Plasma Nitrided Oxides for Ultrathin Gate Dielectric Applications*; SPIE 1998 Symp. Microelec. Manf.; September 1998; Santa Clara, CA; pp 1-11.

Wu et al.; *Improvement of Gate Dielectric Reliability for p+ Poly MOS Devices Using Remote PECVD Top Nitride Deposition on Thin Gate Oxides*; IEEE 98 36th Annual International Reliability Physics Symposium; Reno, Nevada; 1998; pp 70-75.

Chatterjee et al.; *Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process*; Semiconductor Process and Device Center, Texas Instruments; 1997 IEEE; 4 pgs.

Kraft et al.; *Surface nitridation of silicon dioxide with a high density nitrogen plasma*; J. Vac. Sci. Technol. B, Vol. 15, No. 4; 1997 American Vacuum Society; July/August 1997; pp. 967-970.

Jeon et al.; *Low Temperature Preparation of SiO₂ Films With Low Interface Trap Density Using ECR Diffusion and ECR CVD Methods*; 1996 Conference on Optoelectronic and Microelectronic Materials and Devices Proceedings, Canberra, ACT, Australia, 8-11 December 1996; pp. 259-262.

Rau et al.; *Characterization of stacked gate oxides by electron holography*; Appl. Phys. Lett., Vol. 68, No. 24; 1996 American Institute of Physics; 10 June 1996; pp. 3410-3412.

Cramer et al.; *Sodium passivation dependence on phosphorus concentration in tetraethylorthosilicate plasma-enhanced chemical vapor deposited phosphosilicate glasses*; J. Appl. Phys. Vol. 73, No. 5; 1993 American Institute of Physics; 1 March 1993; pp. 2458-2461.

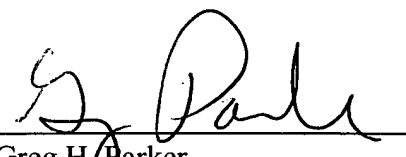
Wolf; *Silicon Processing For The VLSI Era; Volume 2: Process Integration*; Lattice Press, Sunset Beach, California; 1990; pp. 354-361.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above patents and to question the relevance and materiality of the patents listed herein, in whole, in part or in combination, subsequent to filing this Information Disclosure Statement.

A check in the amount of \$ 180.00 is enclosed in payment of the filing fee for this communication. However, the Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.


Greg H. Parker
Registration No. 44,995

Date: 11-5-02

Hitt Gaines & Boisbrun, P.C.
P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800